REMARKS

The Office Action dated May 11, 2005 has been received and carefully considered. In this response, claims 1, 36, 44 and 54 have been amended. Support for these amendments may be found in the specification and drawings as originally filed. Entry thereof and reconsideration of the outstanding rejections in the present application is respectfully requested.

Objection to Claims 9 and 15

At page 2 of the Office Action, claims 9 and 15 were objected to as allegedly having too many unnecessary commas thereby creating confusion and complicating the claim language. However, the Applicants respectfully submit that the number and usage of commas in claims 9 and 15 are entirely consistent with English writing standards. Moreover the use of the commas in claim 9 and 15 do not complicate or create confusion as to the subject matter of claims 9 and 15. Accordingly, the withdrawal of the objection to claims 9 and 15 is respectfully requested.

Anticipation Rejection of Claims 1-8, 13, 19, 20, 36-38, 44, 45, 47, 48 and 52-54

At page 2 of the Office Action, claims 1-8, 13, 19, 20, 36-38, 44, 45, 47, 48 and 52-54 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Mirov (U.S. Patent No. 6,691,215 B1). This rejection is respectfully traversed.

Claim 1, from which claims 2-23 depend, has been amended to recite the features of disabling a phase locked loop by reducing power used for driving the phase locked looped and providing an oscillator signal to drive a clock line when in a first power mode. Claim 36, from which claims 37-42 depend, and claim 44, from which claims 45-54 depend, have been similarly amended. Support for these amendments may be found, *inter alia,* claims 8 and 19 as originally presented. As noted in the response to the previous Office Action, Mirov fails to disclose or suggest disabling a PLL because Mirov merely provides that the PLL may be bypassed through the use of a PLL BYPASS signal. At page 18 of the Office Action, the Examiner asserts that disabling a PLL may be achieved by bypassing the PLL. While the Applicants respectfully disagree, in an effort to advance the present application to issuance, the Applicants have clarified claims 1, 36 and 44 to provide that a phase locked loop is disabled by reducing power used for driving the phase locked loop.

With respect to this clarification, the Examiner asserts with regard to claim 19 that Mirov discloses enabling/disabling the phase locked loop by removing the VCC input of the AND gate 512 in FIG. 7 of Mirov. *See Mirov*, p. 5. The Examiner further relies on col. 11, lines 10-27,

col. 21 lines 47-67, and col. 22 lines 36-67 of Mirov as allegedly disclosing these features. However, contrary to the Examiner's assertions, neither the cited passages of Mirov nor any other passage of Mirov support the Examiner's assertion that Mirov discloses disabling the phase locked loop by reducing power used for driving the phase locked loop as provided by claims 1, 36 and 44. Instead as taught by Mirov at the passage at col. 12 lines 15-23:

> In the illustrated embodiment, the delay circuit 512 takes the form of an AND gate 704 that has a first input coupled to the Clock B signal 412 and a second input tied to a logically high signal, such as system voltage, Vcc. By constructing the AND gates 700 on the same die, using the same processes, and using transistors of similar size and configuration, the delays introduced by the AND gates 700, 704 may be substantially matched.

Thus, rather than reducing power used to drive the phase locked loop of Mirov, the delay circuit 512 "introduces a delay substantially similar to the delay, D1." *Mirov*, col. 12, lines 14-15. One of ordinary skill in the art will appreciate that activating or deactivating the output of the AND gate 704 does not reduce power used to drive any of the components of the PLL 502. As illustrated by FIG. 7 of Mirov, the output of the AND gate 704 is supplied merely as an input to the mixer 504 which, as disclosed by Mirov, introduces a delay substantially similar to the delay D1 introduced by AND gate 700. No passage of Mirov discloses that the use of the delay circuit 512 reduces in any way power used for driving the phase locked loop.

Moreover, the Examiner refers to the passage of Mirov at col. 21, line 27 to col. 23, line 56 in support of the Examiner's assertion that Mirov teaches "a power supply comprised of power modules and method of providing reduced power in comparison to available power to the device" and "enabling/disabling the power modules to produce desired voltage and make available the desired current on a line of different operating modes *Office Action*, p.4. While the Applicants agree with the Examiner that Mirov teaches "a method of providing reduced power" in that Mirov teaches that the power modules 1904, 1906 and 1908 of a power supply 1800 can be selectively disabled to provide reduced power to the computer system 200 (*see, e.g., Mirov*, col. 22, lines 24-34 and FIG. 19), the Applicants respectfully submit that Mirov provides no disclosure that the provision of a reduced amount of power the system results in a reduction of the power supplied to the PLL in any way, and, as will be appreciated by those skilled in the art, the reduction in the total amount of power provided by the power supply 1800 to the computer system 200 does not necessarily require that the power supplied to the PLL be reduced.

Moreover, even if Mirov disclosed a reduction in the power supplied to the PLL (which Mirov does not), Mirov provides no disclosure that a reduction in power contemplated by Mirov would disable the PLL and one of ordinary skill in the art will appreciate that a reduction in power supplied to a PLL does not necessarily disable a PLL.

As described above, Mirov fails to disclose or suggest disabling a PLL by reducing power to the PLL and therefore fails to disclose the features of disabling a phase locked loop by reducing power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode as recited by claim 1 and similar features recited by claim 36 and 44. Accordingly, it is respectfully submitted that the Office Action fails to establish that Mirov discloses each and every feature of claims 1, 36 and 44, as well as each and every feature of claims 2-23, 37-43 and 45-54 at least by virtue of their dependency from one of claims 1, 36 or 44. Moreover, these claims recite additional features not disclosed by Mirov.

In view of the foregoing, it is respectfully submitted that the anticipation rejection is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejections of Claims 1-23 and 36-54

At page 6 of the Office Action, claim 14 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov. At page 7 of the Office Action, claims 1-8, 13, 19-20, 37-38, 44, 45, 47, 48 and 52-54 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann (US Patent No. 5,877,656). At page 10 of the Office Action, claims 9-12, 15-18, 39, 40 and 46 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann and further review of Zhang (US Patent No. 6,687,322). At page 13 of the Office Action, claims 21, 22, 41, 43, and 48-50 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view Durham (US Patent No. 6,785,829). At page 15 of the Office Action claims 23, 42 and 51 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann and further in view of Anwyl (US Patent #5,576,738). These rejections are respectfully traversed.

As discussed above, Mirov fails to disclose or suggest the features of disabling a phase locked loop by reducing power used for driving the phase locked loop and providing an oscillator signal to drive a clock line within a first power mode as provided by claims 1, 36 and 44. The Office Action does not assert that the proposed combinations of Mann, Zhang, Durham and Anwyl disclose or suggest these features. Accordingly, the Office Action fails to establish

that the proposed combinations of Mirov, Mann, Durham, Zhang and Anwyl necessarily disclose or suggest each and every feature of claims 1, 36 and 44, as well as each and every feature of claims 2-23, 37-43 and 45-54 at least by virtue of their dependency from one of claims 1, 36 or 44. Moreover, these claims recite additional features neither disclosed nor suggested by the cited references.

For example, claims 9 and 15, recite the additional features of wherein disabling the phase locked loop further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data. With respect to claim 9, the Examiner asserts that Mirov discloses:

> Mirov discloses an apparatus and method for reducing power consumption comprising: determining (based on the bits) a power mode [power mode] for a device [col. 17, 18-40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]

However, the Applicants respectfully submit that the subject matter of claim 9 is not directed to "determining (based on the bits) a power mode for a device" as the Examiner erroneously contends. Instead, claims 9 and 15 provide that disabling the phase locked loop includes reducing a number of bits used to represent multimedia data. The Office Action does not address how any of the cited references disclose or suggest reducing a number of bits used to represent a multimedia data, nor do any of the cited references in fact teach or disclose these features. Accordingly the Office Action fails to establish that any of the cited references disclose or suggest the additional features of claims 9 or 15. The Office Action also fails to establish that any of the cited references disclose or suggest, alone or in combination, the additional features recited by claim 38 for similar reasons.

In view of the foregoing, it is respectfully submitted that the obvious rejections of claims 1-23 and 36-54 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Conclusion

It is respectfully submitted that the present application is in condition for allowance and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite

resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

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Date

Ryan S. Davidson, Reg. No. 51,596,
TOLER, LARSON & ABEL, L.L.P.
5000 Plaza On The Lake, Suite 265
Austin, Texas 78746
(512) 327-5515 (phone)
(512) 327-5452 (fax)